IN THE CLAIMS:

Please amend claims 1-6 and 9-15. Please cancel claims 7 and 8 without prejudice or disclaimer. Please note that all claims currently pending and under consideration in the above-referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for manufacturing an interconnect structure consisting essentially of:

forming a recess within a dielectric material situated on a semiconductor substrate, the recess extending below a top surface of the dielectric material;

forming a diffusion barrier layer substantially conformally on the top surface of the dielectric material and over an interior surface of the recess;

forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer comprising a material having a melting point greater than or equal to that of a material comprising the seed ~~layer~~ layer, wherein the material comprising the seed layer consists of aluminum, titanium nitride, titanium, or titanium aluminide;

forming an electrically conductive layer on the seed layer over the top surface of the dielectric material and within the recess, the material comprising the diffusion barrier layer having a melting point greater than that of a material comprising the electrically conductive layer, the material comprising the seed layer having a melting point greater than or equal to that of the material comprising the electrically conductive layer;

forming an energy absorbing layer on the electrically conductive layer, the energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

~~applying, omnidirectionally,~~ applying energy to the energy absorbing layer sufficient to cause the electrically conductive layer to flow within the recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein forming a diffusion barrier layer ~~on the recess within the dielectric material is effected by CVD~~comprises forming the diffusion barrier layer by chemical vapor deposition.

3. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein forming a diffusion barrier layer comprises forming the ~~material comprising the~~ diffusion barrier layer from a material ~~is~~ selected from the group consisting of ceramics, metallics, and intermetallics.

4. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein forming a diffusion barrier layer comprises forming ~~the material comprising~~ the diffusion barrier layer ~~is~~ from a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, further comprising, prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing a nitrogen gas.

6. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein ~~depositing~~ forming a seed layer on the diffusion barrier layer ~~is effected by CVD~~ comprises depositing the seed layer by chemical vapor deposition.

Claims 7 and 8 (Canceled)

9. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure~~

~~as recited in Claim 1~~ of claim 1, wherein forming an electrically conductive layer comprises forming the electrically conductive layer from a ~~the~~ material ~~comprising the electrically conductive layer is~~ selected from the group consisting of aluminum and copper.

10. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein forming an energy absorbing layer comprises forming the energy absorbing layer ~~comprises~~ from a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~of claim 1, wherein applying energy to the energy absorbing layer comprises applying the energy to the energy absorbing layer ~~utilizes~~ utilizing a furnace.

12. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer comprises removing the portions of the energy absorbing layer and the electrically conductive layer by abrasive planarization.

13. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 12~~ of claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer comprises removing the portions of the energy absorbing layer and the electrically conductive layer by chemical mechanical planarization.

14. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, further comprising forming the recess to have an aspect ratio greater than about four (4) to one (1).

15. (Currently Amended) ~~A~~ The method ~~for manufacturing an interconnect structure as recited in Claim 1~~ of claim 1, further comprising forming the recess to comprise a contact hole situated below a trench, the contact hole terminating at an end thereof at the semiconductor substrate and terminating at an opposite end thereof at the trench, the trench extending from the opposite end of the contact hole to the top surface of the dielectric material, the trench extending parallel to the plane of the semiconductor substrate.

Claims 16-63 (Canceled)